

13A, 500V N-CHANNEL MOSFET

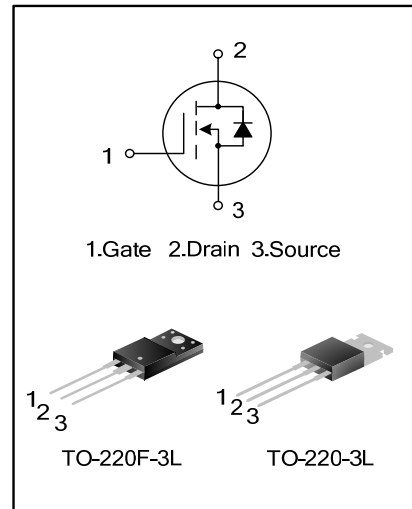
GENERAL DESCRIPTION

SVD13N50T/F is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary S-Rin™ structure DMOS technology. The improved planar stripe cell and the improved guarding ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.

FEATURES

- * 13A,500V,RDS(on)(typ)=0.36Ω@VGS=10V
- * Low gate charge
- * Low Crss
- * Fast switching
- * Improved dv/dt capability



ORDERING SPECIFICATIONS

Part No.	Package	Marking	Material	Packing
SVD13N50T	TO-220-3L	SVD13N50T	Pb free	Tube
SVD13N50F	TO-220F-3L	SVD13N50F	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS (Tc=25°C unless otherwise noted)

Parameter	Symbol	Rating		Unit
		SVD13N50T	SVD13N50F	
Drain-Source Voltage	VDS	500		V
Gate-Source Voltage	VGS	±30		V
Drain Current	ID	13		A
Power Dissipation(Tc=25°C)	PD	180	51	W
Single Pulsed Avalanche Energy (Note 1)	EAS	1446		mJ
Operation Junction Temperature	TJ	150		°C
Storage Temperature	Tstg	-55~+150		°C

THERMAL CHARACTERISTICS

Parameter	Symbol	Rating		Unit
		SVD13N50T	SVD13N50F	
Thermal Resistance, Junction-to-Case	R θ JC	1.25	5	°C/W
Thermal Resistance, Junction-to-Ambient	R θ JA	62.5	120	°C/W

ELECTRICAL CHARACTERISTICS (T_c=25°C unless otherwise noted)

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BVDSS	VGS=0V, ID=250 μ A	500	--	--	V
Drain-Source Leakage Current	IDSS	VDS=650V, VGS=0V	--	--	1	μ A
Gate-Source Leakage Current	IGSS	VGS= \pm 30V, VDS=0V	--	--	\pm 100	nA
Gate Threshold Voltage	VGS(th)	VGS= VDS, ID=250 μ A	2.0	--	4.0	V
Static Drain- Source On State Resistance	RDS(on)	VGS=10V, ID=6.5A	--	0.36	0.52	Ω
Input Capacitance	Ciss	VDS=25V, VGS=0V, f=1.0MHZ	--	1838	--	pF
Output Capacitance	Coss		--	194	--	
Reverse Transfer Capacitance	Crss		--	10.6	--	
Turn-on Delay Time	td(on)	VDD=250V, ID=6.5A, RG=4.7 Ω , VGS=10V (Note 2,3)	--	52	--	ns
Turn-on Rise Time	tr		--	40	--	
Turn-off Delay Time	td(off)		--	352	--	
Turn-off Fall Time	tf		--	40	--	
Total Gate Charge	Qg	VDS=400V, ID=13A, VGS=10V (Note 2,3)	--	53.18	--	nC
Gate-Source Charge	Qgs		--	11.08	--	
Gate-Drain Charge	Qgd		--	17.17	--	

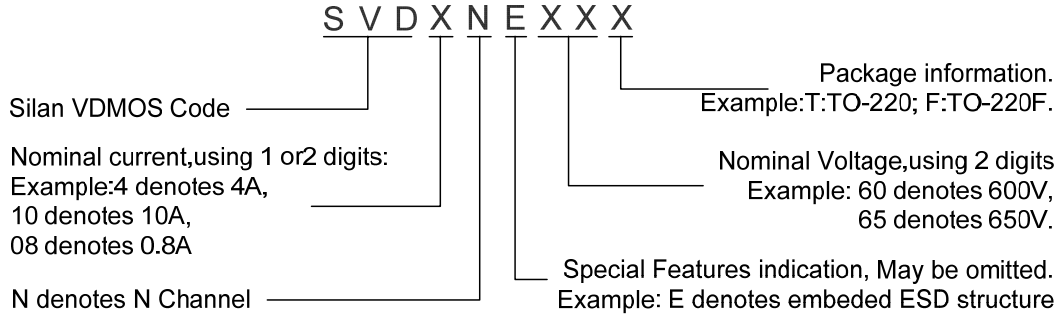
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	IS	Integral Reverse p-n Junction Diode in the MOSFET	--	--	13	A
Pulsed Source Current	ISM		--	--	52	
Diode Forward Voltage	VSD	IS=13A, VGS=0V	--	--	1.4	V
Reverse Recovery Time	Trr	IS=13A, VGS=0V, dIF/dt=100A/ μ S (Note 2)	--	450	--	ns
Reverse Recovery Charge	Qrr		--	5.0	--	μ C

Notes:

- L=30mH, IAS=7.725A, VDD=250V, RG=25 Ω , starting T_J=25°C;
- Pulse Test: Pulse width \leq 300 μ s, Duty cycle \leq 2%;
- Essentially independent of operating temperature.

NOMENCLATURE



TYPICAL CHARACTERISTICS

Figure 1. On-region characteristics

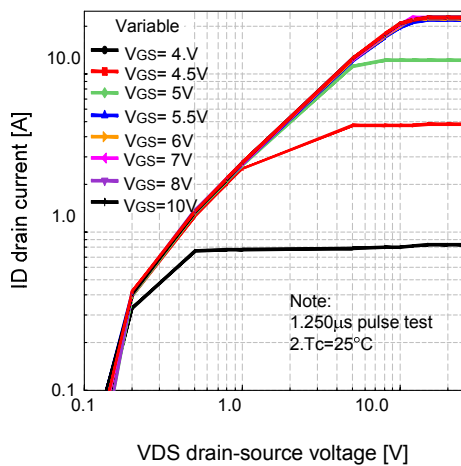


Figure 2. Transfer characteristics

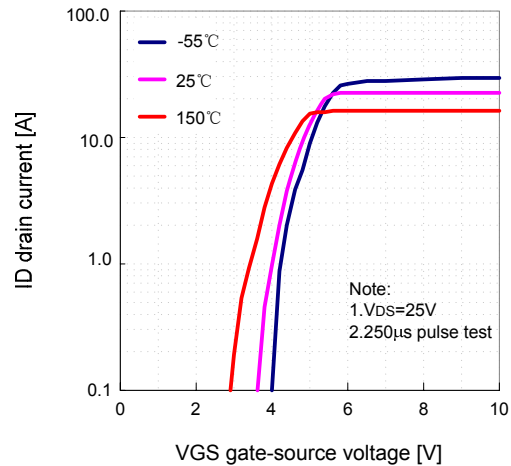


Figure 3. On-resistance variation vs. drain current and gate voltage

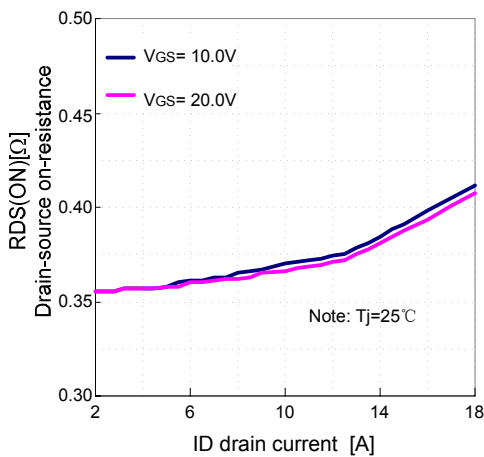
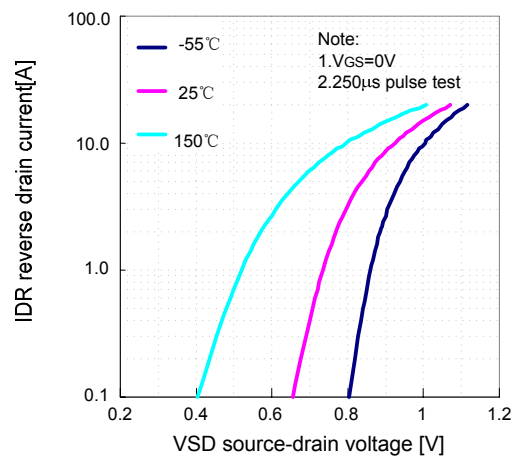


Figure 4. Body diode forward voltage variation vs. source current



TYPICAL CHARACTERISTICS(continued)

Figure 5. capacitance characteristics

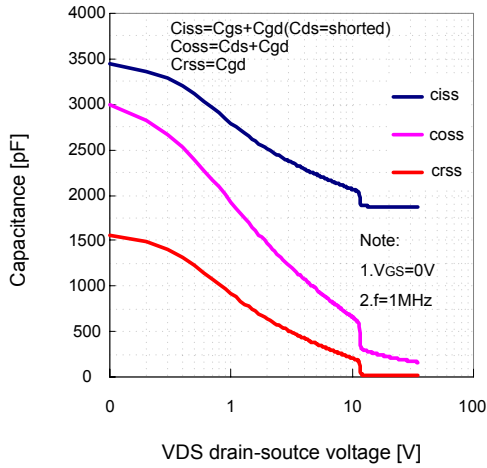


Figure 6. gate charge characteristics

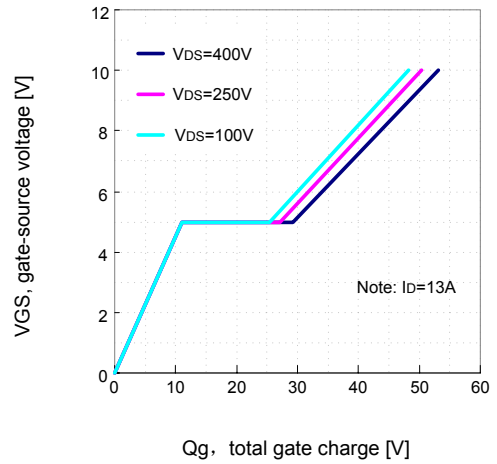


Figure 7. breakdown voltage variation vs. temperature

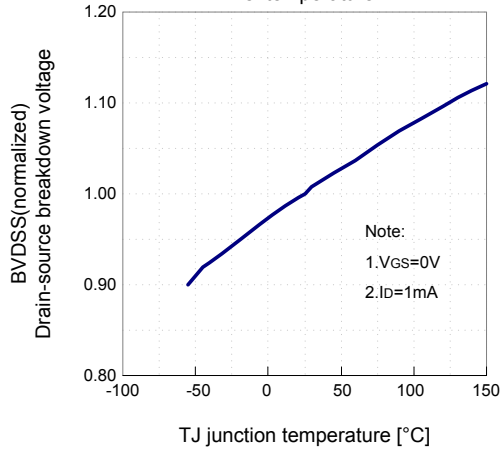
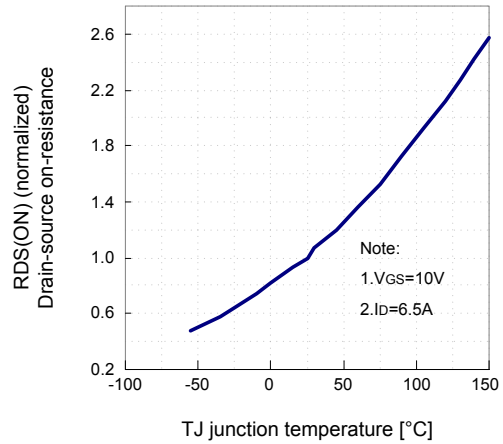
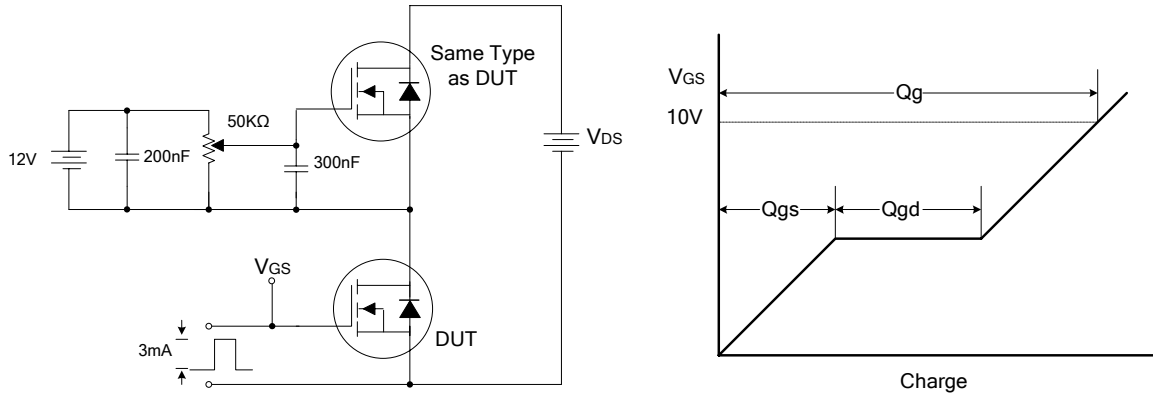


Figure 8. on-resistance variation vs. temperature

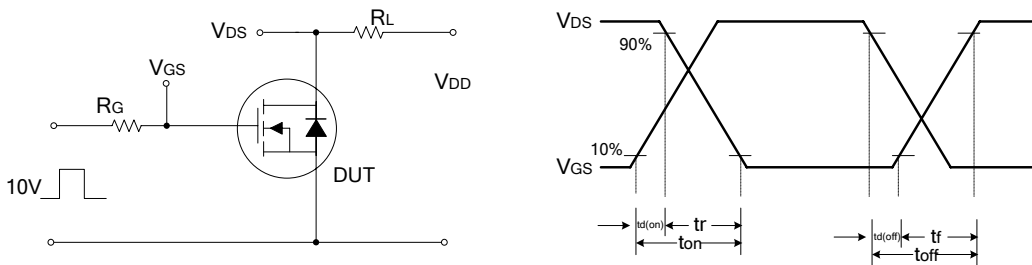


TYPICAL TEST CIRCUIT

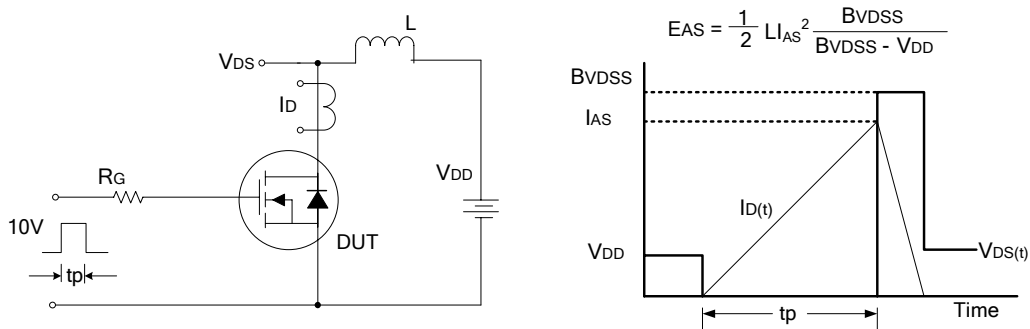
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



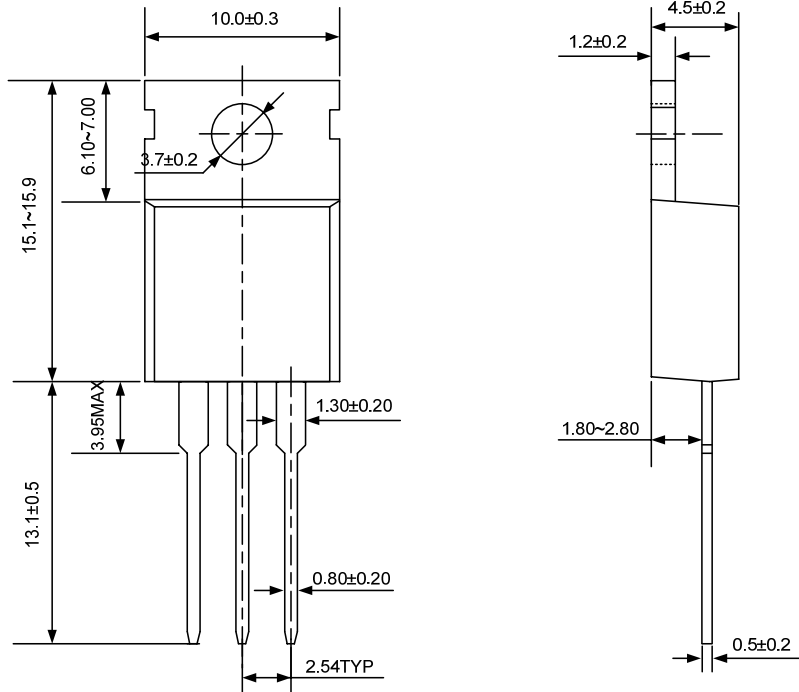
Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

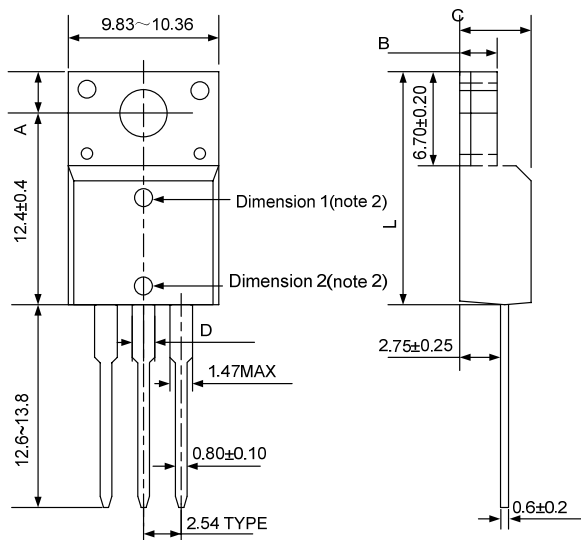
TO-220-3L

UNIT: mm



TO-220F-3L

UNIT: mm



Symbol(note1)	Dimension1	Dimension2
A	3.30 ± 0.15	2.70 ± 0.15
B	2.55 ± 0.20	3.0 ± 0.20
C	4.72 ± 0.2	4.50 ± 0.20
D	1.47 MAX	1.75 MAX
L	15.75 ± 0.30	15.00 ± 0.30

Note1: There may be two values for some products due to different plastic mould machine, so two dimensions of the same position are listed;
 Note2: When the product size is Dimension1, the thimble hole is on top of the surface; when the size is Dimension2, the center hole is on bottom of the surface.



Disclaimer:

- Silan reserves the right to make changes to the information herein for the improvement of the design and performance without further notice! Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current.
- All semiconductor products malfunction or fail with some probability under special conditions. When using Silan products in system design or complete machine manufacturing, it is the responsibility of the buyer to comply with the safety standards strictly and take essential measures to avoid situations in which a malfunction or failure of such Silan products could cause loss of body injury or damage to property.
- Silan will supply the best possible product for customers!



ATTACHMENT

Revision History

Date	REV	Description	Page
2010.05.14	1.0	Original	
2010.10.21	1.1	Modify" ORDERING SPECIFICATIONS", the parameters, the template of Datasheet	